IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): K.L. Davison et al.
Case: 4-7-23
Serial No.: 10/722,652
Filing Date: November 26, 2003
Group: 2831
Examiner: Hung V. Ngo

Title: Methods and Apparatus for Integrated Circuit Device Power Distribution via Internal Wire Bonds

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TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

(1) Appeal Brief; and
(2) Copy of Notice of Appeal, filed on April 26, 2005, with copy of stamped return postcard indicating receipt of Notice by PTO on April 29, 2005.

Please extend the period for response by one month to July 29, 2005. Please charge **Ryan, Mason & Lewis, LLP Account No. 50-0762** the amount of $620 ($500 to cover this submission under 37 CFR §1.17(c) and $120 to cover the one month extension fee). In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully submitted,

Robert W. Griffith

Date: June 30, 2005

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

Applicants (hereinafter referred to as "Appellants") hereby appeal the final rejection of claims 1-28 of the above referenced application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

Claims 1-20 are pending in the present application. Claims 10 and 12 are allowable. Claims 1-9, 11 and 13-20 stand rejected under 35 U.S.C. §102(e) and are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides techniques for power distribution within an integrated circuit device that reduces the voltage drop typically associated with conventional power distribution in such devices (Specification, page 3, lines 8-10).

Claim 1 provides an integrated circuit device having a die. Bond pads are disposed in a peripheral region of the die and one or more internal power buses are disposed in an interior region of the die. The one or more internal buses distribute power to internal node points of the die. One or more bond wires connect one or more of the peripheral bond pads with one or more internal buses.

By way of example, illustrative embodiments of the invention of claim 1 are shown in FIGS. 1 and 2 of the drawings. FIG. 1 shows a top view of an integrated circuit device 100 with positive voltage supply bond pads 104 and negative voltage supply bond pads 106 shared by internal bond wires 116 and external bond wires 112 for power distribution through the integrated circuit device 100. FIG. 2 shows a top view of an integrated circuit device 200 having positive voltage supply bond pads 204 and negative voltage supply bond pads 206 for external bond wires 212 and additional positive voltage supply bond pads 205 and negative voltage supply bond pads 207 for internal bond wires 216 for power distribution through the integrated circuit device 200.

Claim 20 provides a method of constructing an integrated circuit device. An integrated circuit die is formed having at least one peripheral bond pad and at least one internal bus. The at least one peripheral bond pad is wire bonded to the at least one internal bus.

By way of example, an illustrative embodiment of the invention of claim 20 is shown in FIG. 3. FIG. 3 is a flow diagram illustrating the manner in which an integrated circuit device 100, 200 is constructed utilizing internal wire bonds 116, 216 for power distribution.

Advantageously, the present invention in the illustrative embodiments provides techniques for distributing power through an integrated circuit device in which bond wires are utilized for connecting the positive voltage supply and negative voltage supply from the periphery to internal buses. Wire bonding is a relatively inexpensive process that allows for sufficient transmission of power to interior regions of the die of the integrated circuit device without increasing the number of metal layers. Further, bond wires provide lower resistivity than traditional metal lines. Thus, the use of internal wire bonding as disclosed herein substantially reduces the power distribution voltage drop that normally occurs in metal lines routed from the bond pads to the internal buses of the integrated circuit device (Specification, page 9, lines 19-27).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-9, 11 and 13-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,727,597 to Taylor et al. (hereinafter "Taylor").

ARGUMENT

Appellants incorporate by reference herein the disclosures of all previous responses filed in the present application, namely, responses dated October 29, 2004 and April 26, 2005.

A. Claims 1-8, 14, 15 and 17-19

Independent claim 1 of the present invention recites an integrated circuit device with a die having a peripheral region and an interior region on its top surface. A plurality of bond pads are disposed in the peripheral region of the die, and at least one internal bus is disposed in the interior region of the die. The internal bus distributes power to a plurality of internal node points of the die. At least one bond wire connects at least one of the plurality of bond pads with the at least one internal bus.

Taylor discloses an integrated circuit device having C4 (controlled collapse chip) pads and wire bond pads. Each of the C4 pads is electrically coupled through metal layers and conductive vias to one of the wire bond pads located near the periphery of the integrated circuit device. C4 power connections and ground connections are electrically coupled by traces to one or more wire bond pad

power and ground connections, respectively. In order to provide a pad layout that makes it easier to route the electrical connections between the pads, the C4 pads are placed in alignment with the wire bond pads.

Taylor fails to disclose at least one bond wire connecting at least one of a plurality of bond pads, disposed in a peripheral region of the die, with at least one internal bus, disposed in an interior region of the die, as recited in independent claim 1. On page 3 of the final Office Action, the Examiner contends that "Taylor et al disclose at least one bond wire (Fig. 3b) connecting at least one of the plurality of bond pads (304) with the at least one internal bus (360)." Appellants assume that the Examiner is actually referring to FIG. 3C, which shows a cross-sectional side view of an integrated circuit and a possible wire bond connection. However, in column 2, lines 49-52, Taylor states, "integrated circuit device 300 may be electrically coupled to a package 360 (shown in FIG. 3C) by either of wire bond pads 304, or C4 pads 306." Thus, element 360 of FIG. 3B represents a power bus, while element 360 of FIG. 3C represents a package. It is apparent that Taylor inadvertently used the same reference numeral, that is, reference numeral 360, to refer to two entirely different structures, a power bus and a package. The Examiner, in formulating the rejection, is relying on a wire bond connection between a bond pad and a package. This is further supported by the fact that element 360 of FIG. 3C is not shown as part of integrated circuit device 300 as it is in FIG. 3B. Thus, assuming *arguendo*, that FIG. 3C of Taylor shows a bond wire (not described in the specification) connecting elements 304 and 360, the respective elements are described as a wire bond pad and a package, and thus, Taylor fails to disclose a bond wire connecting a bond pad with an internal bus.

Additionally, in column 2, lines 64-65, Taylor specifically states that "wire bond pads 304 are coupled to the C4 pads 306 through the metal layers 330 and conductive vias 332." Further, in column 3, lines 48-50, Taylor discloses that "the wire bond power connections 350 are coupled to the C4 power buses 360 along a metal trace connecting two of the C4 power connections 340." Therefore, the disclosure of a trace connection instead of a wire bond connection directly teaches away from the invention recited in claim 1 of the present invention.

Dependent claims 2-8, 14, 15, 17 and 18 are patentable at least by virtue of their dependency from independent claim 1. The patentability of independent claim 1 is described above. Dependent claims 2-8, 14, 15, 17 and 18 also recite patentable subject matter in their own right.

Independent claim 19 recites a die configurable for use in an integrated circuit device having a plurality of bond pads disposed in the peripheral region of the die, and at least one internal bus disposed in the interior region of the die that distributes power to a plurality of internal node points of the die. The plurality of bond pads and the at least one internal bus are connectable by at least one bond wire. Taylor fails to disclose a die having a bond pad and an internal bus connectable by at least one bond wire. Additionally, independent claim 19 is patentable for reasons similar to those presented above with regard to independent claim 1.

B. Claim 9

Dependent claim 9 is patentable at least by virtue of its dependency from independent claim 1. The patentability of claim 1 is described above. However, dependent claim 9 also recites patentable subject matter in its own right. Dependent claim 9 recites an integrated circuit device, as recited in claim 1, in which the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a positive voltage supply terminal of the device.

Appellants initially note that the Examiner, in formulating the §102(e) rejection of this claim, provides no specific arguments as to why this claim is anticipated by Taylor beyond that provided for independent claim 1. In other words, the Examiner does not cite the specific portions of Taylor that allegedly anticipate the particular limitations of this dependent claim. Appellants respectfully submit that this does not meet the specificity requirements for a rejection under the Federal Rules and the MPEP. 37 C.F.R. §§1.104(c)(2) requires:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified. (*emphasis added*)

Moreover, MPEP §706 requires that "[w]hen a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable." The rejection of dependent claim 9 is, therefore, deficient with respect to these requirements. Additionally, Taylor fails to disclose any bond pads wire bonded to an internal bus, and also fails to disclose that these bond pads are also wire bonded via another bond wire to a positive voltage supply terminal of the device.

C. Claim 11

Dependent claim 11 is patentable at least by virtue of its dependency from independent claim 1. The patentability of claim 1 is described above. However, dependent claim 11 also recites patentable subject matter in its own right. Dependent claim 11 recites an integrated circuit device, as recited in claim 1, in which the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a negative voltage supply terminal of the device.

Appellants initially note that the Examiner, in formulating the §102(e) rejection of this claim, provides no specific arguments as to why this claim is anticipated by Taylor beyond that provided for independent claim 1. In other words, the Examiner does not cite the specific portions of Taylor that allegedly anticipate the particular limitations of this dependent claim. Appellants respectfully submit that this does not meet the specificity requirements for a rejection under the Federal Rules and the MPEP. Additionally, Taylor fails to disclose any bond pads wire bonded to an internal bus, and also fails to disclose that these bond pads are also wire bonded via another bond wire to a negative voltage supply terminal of the device.

D. Claim 13

Dependent claim 13 is patentable at least by virtue of its dependency from independent claim 1. The patentability of independent claim 1 is described above. However, dependent claim 13 also recites patentable subject matter in its own right. Dependent claim 13 recites an integrated circuit device, as recited in claim 1, in which the at least one of the plurality of bond pads wire bonded to the at least one internal bus is connected to another of the plurality of bond pads.

Appellants again note that the Examiner, in formulating the §102(e) rejection of this claim, provides no specific arguments as to why this claim is anticipated by Taylor beyond that provided for independent claim 1. In other words, the Examiner does not cite the specific portions of Taylor that allegedly anticipate the particular limitations of this dependent claim. Appellants respectfully submit that this does not meet the specificity requirements for a rejection under the Federal Rules and the MPEP, as described above. Additionally, as described above with regard to claim 1, Taylor fails to disclose bond pads wire bonded to an internal bus. Therefore, Taylor also fails to disclose that these bond pads are connected to other bond pads on the periphery of the die.

E. Claim 16

Dependent claim 16 is patentable at least by virtue of its dependency from independent claim 1. The patentability of independent claim 1 is described above. However, dependent claim 16 also recites patentable subject matter in its own right. Dependent claim 16 recites an integrated circuit device, as recited in claim 1, in which the power is distributed from the at least one of the plurality of bond pads to at least one secondary bond pad through a metal connector, and from the at least one secondary bond pad to the at least one internal bus through at least one wire bond connection within the peripheral region of the die.

Appellants again note that the Examiner, in formulating the §102(e) rejection of this claim, provides no specific arguments as to why this claim is anticipated by Taylor beyond that provided for independent claim 1. In other words, the Examiner does not cite the specific portions of Taylor that allegedly anticipate the particular limitations of this dependent claim. Appellants respectfully submit that this does not meet the specificity requirements for a rejection under the Federal Rules and the MPEP, as described above. Additionally, as described above with regard to claim 1, Taylor fails to disclose bond pads wire bonded to an internal bus. Therefore, Taylor also fails to disclose a power distribution scheme from a first bond pad to a second bond pad through a metal connector, and from the second bond pad to an internal bus through a wire bond connection.

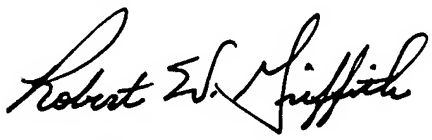
F. Claim 20

Independent claim 20 recites a method of constructing an integrated circuit device. An integrated circuit die is formed having at least one peripheral bond pad and at least one internal bus. The internal bus is configured for distributing power to a plurality of internal node points of the integrated circuit device. The at least one peripheral bond pad is wire bonded to the at least one internal bus.

Appellants note that the Examiner, in formulating the §102(e) rejection of this claim, provides no specific arguments as to why this claim is anticipated by Taylor beyond that provided for independent claim 1. In other words, the Examiner does not cite the specific portions of Taylor that allegedly anticipate the particular limitations of this independent claim. Appellants respectfully submit that this does not meet the specificity requirements for a rejection under the Federal Rules and the MPEP, as described above. Additionally, Appellants assert that there is no disclosure in Taylor of a method of constructing an integrated circuit device. Further, Taylor fails to disclose the step of wire bonding a peripheral bond pad to an internal bus.

For at least the reasons given above, Appellants respectfully request withdrawal of the §102(e) rejection of claims 1-9, 11 and 13-20. Appellants believe that claims 1-9, 11 and 13-20 are patentable over Taylor. As such, the application is believed to be in condition for allowance, and favorable action is respectfully solicited.

Respectfully submitted,



Date: June 30, 2005

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CLAIMS APPENDIX

1. An integrated circuit device comprising:

a die having a top surface with a peripheral region and an interior region surrounded by the peripheral region:

a plurality of bond pads disposed in the peripheral region of the die;

at least one internal bus, disposed in the interior region of the die, that distributes power to a plurality of internal node points of the die; and

at least one bond wire connecting at least one of the plurality of bond pads with the at least one internal bus.

2. The integrated circuit device of claim 1, wherein the at least one internal bus comprises a metal power grid.

3. The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one internal positive voltage supply bus.

4. The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one internal negative voltage supply bus.

5. The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one pair of buses comprising an internal positive voltage supply bus and internal negative voltage supply bus.

6. The integrated circuit device of claim 5, wherein at least one of the voltage supply buses comprises a ground bus.

7. The integrated circuit device of claim 1, wherein the at least one internal bus comprises bond pads having active circuitry disposed thereunder.

8. The integrated circuit device of claim 1, wherein at least one of the plurality of bond pads is wire bonded to an integrated circuit package.

9. The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a positive voltage supply terminal of the device.

11. The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a negative voltage supply terminal of the device.

13. The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is connected to another of the plurality of bond pads.

14. The integrated circuit device of claim 1, further comprising local power interconnects that distribute power from the at least one internal bus to the plurality of internal node points.

15. The integrated circuit device of claim 1, wherein the plurality of internal node points comprise circuit elements.

16. The integrated circuit device of claim 1, wherein the power is distributed from the at least one of the plurality of bond pads to at least one secondary bond pad through a metal connector, and from the at least one secondary bond pad to the at least one internal bus through at least one wire bond connection within the peripheral region of the die.

17. The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads comprises at least one pair of bond pads comprising a positive voltage supply bond pad and a negative voltage supply bond pad.

18. The integrated circuit device of claim 17, wherein the at least one pair of bond pads comprises at least about twelve pairs of bond pads substantially evenly spaced apart in the peripheral region of the die.

19. A die configurable for use in an integrated circuit device, the die having a top surface with a peripheral region and an interior region surrounded by the peripheral region, the die comprising:

a plurality of bond pads disposed in the peripheral region of the die; and

at least one internal bus, disposed in the interior region of the die, that distributes power to a plurality of internal node points of the die;

wherein the plurality of bond pads and the at least one internal bus are connectable by at least one bond wire.

20. A method of constructing an integrated circuit device comprising the following steps:

forming an integrated circuit die having at least one peripheral bond pad and at least one internal bus, the internal bus being configured for distributing power to a plurality of internal node points of the integrated circuit device; and

wire bonding the at least one peripheral bond pad to the at least one internal bus.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.